PATENT ABSTRACTS OF JAPAN

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(54) THIN-FILM TRANSISTOR

(57)Abstract:
PURPOSE: To provide a gate electrode and wiring, where hillocks are hard to occur and which are flat and are easy to be anodized, by adding Cu or Ni to Al.
CONSTITUTION: As the material used for a gate electrode and wiring, an electrode material mainly composed of Al is used, and as an additive metal, Cu and Ni are selected. Cu is effective for electromigration, and Ni has an effect on suppression of hillock generation. As the result of having investigated the surface roughness by the addition of Cu or Ni to Al, which becomes the criteria of hillock, and the value of sheet resistance, which causes signal delay, by experimentation, it was found that Al-1wt.%Cu or Al-3wt.%Ni was much better in surface roughness than an electrode, where Si is added to Al, that the sheet resistance value of Al-1wt.%Cu was much better than Al-1wt.%Si or Al-3wt.% Ni, and that the anode oxide film of Al-1wt.%Cu fulfilled the mechanism as an insulating film enough. Accordingly, it can be flattened by preventing the hillock, using an At-Cu material, where 1% Cu is added to Al, for a gate electrode or wiring.

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CLAIMS

[Claim(s)]
[Claim 1] The gate electrode and gate wiring which consist of aluminum by which Cu or nickel partially prepared on the insulating substrate and this insulating substrate was added, The 1st insulating layer which anodized the front face of this gate electrode, and the 2nd insulating layer prepared on said insulating substrate so that this 1st insulating layer might be covered, The thin film transistor characterized by having the semi-conductor layer prepared on this 2nd insulating layer, and the source field and drain field prepared on this semi-conductor layer so that the both sides of this gate electrode might be met.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the thin film transistor (it is called Following TFT) of reverse stagger structure used for a liquid crystal display panel etc.
[0002]
[Description of the Prior Art] Conventionally, as a gate electrode of TFT, it has been conditions that an adhesive property with a substrate is good, that there is no irregularity by which it is called a hillock to a front face, and not to deteriorate in the process which forms SiN which is gate dielectric film, and Cr film is used. On the other hand as gate wiring, the low thing of resistance serves as conditions, and it is not suitable to divert Cr film with the high rate of specific resistance. Therefore, the two-layer film on which aluminum film with the rate of specific resistance lower single or more figures than Cr was put is used on Cr film.
[0003] However, when structure which is different in the gate electrode of TFT and wiring in this way is applied, there is a trouble of bringing about the increment in a patterning routing counter, i.e., a mask process.
[0004] Then, as shown in JP,2-85826,A, aluminum or aluminum-Si, and aluminum-Pd are used for a gate electrode and wiring, and the approach of anodizing this gate electrode and wiring, and forming gate dielectric film, such as SiN, by plasma CVD some gate dielectric film, nothing, and after that is proposed.
[0005]
[Problem(s) to be Solved by the Invention] However, there is a problem as shown below in aluminum, aluminum-Si, and aluminum-Pd which are used for a gate electrode.
[0006] it is easy to generate the irregularity which is alike and is called a hillock, and irregularity generates aluminum also into the part of the channel formed through the insulating material on the gate electrode by this hillock. And there is a problem that the distance to which an electron moves a channel in the part of this irregularity becomes long, electron mobility falls and the switching rate of TFT becomes slow by that cause.
[0007] Although a hillock cannot generate aluminum-Si easily compared with aluminum, when Si is not etched in the part where the aluminum-Si film should be removed in the patterning process after forming aluminum-Si, but it remains and the pixel for a display is formed as it was, this may short-circuit wiring of signal I/O and there is a problem that it does not function as a pixel for a display.
[0008] If aluminum-Pd remains as it is that Pd is hard to anodize and SiN and a-Si are formed by the plasma-CVD method on it, withstand voltage will fall in the part of Pd which did not oxidize, a gate electrode and wiring, and other electrodes and wiring will short-circuit, and the trouble of not functioning as a transistor or becoming the cause of failure will be got. Therefore, when these metallic materials are used for a gate electrode and wiring, the problem that the yield will become the bad thing which has low dependability as a thin film transistor of reverse stagger structure occurs.
[0009] Then, this invention offers the gate electrode and wiring which is easy to ********** among flatness that it is hard to generate a hillock in view of the above-mentioned trouble.
[0010]
[Means for Solving the Problem] namely, in the thin film transistor of this invention made in order to solve the above-mentioned technical problem The gate electrode and gate wiring which consist of aluminum by which Cu or nickel partially prepared on the insulating substrate and this insulating substrate was added, The 1st insulating layer which anodized the front face of this gate electrode, and the 2nd insulating layer prepared on said insulating substrate so that this 1st insulating layer might be covered, It is characterized by having the semi-conductor layer prepared on this 2nd insulating layer, and the source field and drain field prepared on this semi-conductor layer so that the both sides of this gate electrode might be met.
[0011]
[Example] The gate electrode and wiring material of the thin film transistor which is one example of this invention are explained below.
[0012] First, it decided to use the electrode material which makes a subject aluminum with the rate of specific resistance small as usual as an ingredient used for a gate electrode and wiring. And Cu and nickel were chosen as an addition metal to aluminum. This is explained below.
[0013] Usually, although a current will occur by electronic flow if an electrical potential difference is built over an electrode and wiring, in aluminum electrode and wiring, migration of aluminum ion will also participate in a current besides electronic flow. An electrode or wiring may become extinct by migration of this aluminum ion. Although this is called electromigration, it is known that Cu is effective to this electromigration.
[0014] Moreover, it is known that effectiveness is in hillock generating suppression in nickel. Next, the sheet resistance constituting the surface roughness by the addition to aluminum which serves as a standard of a hillock about them, and the cause of signal delay was investigated. The results of an investigation are shown in Table 1 with the results of an investigation of aluminum and aluminum-Si (Si1%) which are mentioned to said JP,2-85826,A. in addition, the investigated ingredient — aluminum — pure — aluminum-1wt% by which aluminum and Si were added 1% — aluminum-1wt% by which Si and Cu were added 1% — Cu and nickel are aluminum-3wt%nickel added 3%.
[0015]

[Table 1]

	純Al	Al-1wt%Si	Al-1wt%Cu	Al-3wt%Ni
平均表面粗さ Ra (nm)	13.1	9.5	2.6	3.8
シート抵抗) (膜厚200nm (Ω/□)	0.19	0.54	0.29	0.53

As opposed to surface roughness being 9.5nm in 13.1nm and aluminum-1wt%Si with pure aluminum according to this table 1 in aluminum-1wt%Cu 2.6nm, With aluminum-3wt%nickel, it was set to 3.8nm, and surface roughness was obtained rather than the thing of only pure aluminum, and, as for aluminum-1wt%Cu, 4 and a very flat surface of metal were acquired about 1/rather than the thing of only about 1/5 and aluminum-1wt%Si. Moreover, also in aluminum-3wt%nickel, as for surface roughness, the thing of only pure aluminum shows that it is very small with two fifths rather than the thing of only about 3/10 and aluminum-1wt%Si. Thereby, it can be said that the electrode which added Cu or nickel to aluminum is very better for the electrode of only aluminum, or aluminum than the electrode which added Si.

[0016] Moreover, it can be said that aluminum-1wt%Cu becomes about about 1.5 times about sheet resistance, and there is almost no difference compared with aluminum. Moreover, although aluminum-1wt%Si and aluminum-3wt%nickel are almost comparable and become about 3.6 times and a large value compared with pure aluminum, since they are not that single figures also differ, it can be considered that they are a value also with almost sufficient aluminum-3wt%nickel. increase of this sheet resistance -- CuAl2 etc. -- it thinks for increase of the resistivity by formation and impurity scattering of a compound. Therefore, although aluminum-1wt%Si, aluminum-3wt% nickel, and aluminum-1wt%Cu are inferior compared with pure aluminum, respectively about sheet resistance, it can be considered that it is practically not much satisfactory. Since especially the sheet resistance of aluminum-1wt%Cu showed the value quite near the sheet resistance of aluminum, compared with aluminum-1wt%Si and aluminum-3wt%nickel, it can be said that it is very good.

[0017] Based on the above result, the optimal addition of Cu added to aluminum next was investigated. The result is shown in drawing 2 . The aluminum-Cu thickness at this time could be 200nm. The times of Cu of surface roughness being 1% from this drawing are 2.6nm and best. Moreover, it turns out that sheet resistance becomes large along with the increment in an addition. Therefore, the optimal addition with which surface roughness fills two requests that it is small and sheet resistance is also small becomes 1%. although the sheet resistance at this time becomes large slightly with 1.5 times in the case of pure aluminum as aforementioned, it becomes a problem practically as a wiring material -- like .

[0018] Next, the insulating property of the film which anodized the aluminum-1wt%Cu thin film which added Cu 1% to aluminum was investigated. The result is shown in drawing 3 . It is SiNX by plasma CVD on the film which anodized the aluminum-1wt%Cu thin film, and the oxide film on anode of aluminum. The thing on which the film was made to deposit, respectively, and SiNX An insulating property with a membranous thing is shown in drawing 3 as properties X, Y, and Z, respectively. The water solution which neutralized the 0.1M adipic acid to pH 7.0**0.5 with aqueous ammonia was used for anodization liquid. Thickness presupposed that it is fixed 400nm. Although X was a little inferior to this drawing compared with Y, compared with Z, the property with about single sufficient figure was acquired. Thereby, it can be said that the oxide film on anode of aluminum-1wt%Cu fully achieves the function as an insulator layer.

[0019] Thus, if aluminum-1wt%Cu which added Cu 1% is used for aluminum as a gate electrode, it will be very flat and an electrode also with sufficiently low resistance will be obtained. Moreover, this aluminum-1wt%Cu is anodized and it is SiNX on it. Insulating property also with the sufficient gate dielectric film on which the film was made to deposit is shown.

[0020] as mentioned above, the gate electrode with which the flat electrode surface which a hillock does not generate is acquired and it is easy to anodize it -- low -- dependability can offer the good thin film transistor of the yield more high again by using for a gate electrode and wiring the aluminum-Cu ingredient which added Cu 1% to aluminum which serves as gate wiring [****].

[0021] The example of 1 production process of the thin film transistor using the above-mentioned gate electrode and wiring material is shown briefly [drawing 1] below. In addition, although gate wiring is not shown in this drawing, patterning is carried out to coincidence at the time of patterning of a gate electrode.

[0022] aluminum-1wt%Cu by which Cu used as the gate electrode 8 was added by the glass substrate 9 1% is deposited, and patterning is carried out to a desired pattern. The front face of the gate electrode 8 by which patterning was carried out is anodized with the water solution which neutralized the 0.1M adipic acid to pH 7.0**0.5 with aqueous ammonia, and an oxide film on anode 7 is formed. Since anodic oxidation liquid will turn to the bottom of it even if dust exists on the gate electrode 8, this anodic oxidation can form certainly the oxide film on anode 7 used as an insulator layer. Continuation membrane formation of the a-Si film 5 used as the insulator layer 6 and channel which consist of SiN on an anodized film 7, and the protective coat 3 which consists of SiN further is carried out by plasma CVD. And patterning only of the protective coat 3 is carried out. This protective coat 3 carries out the role which protects the a-Si film 5 which is a channel layer from the etchant at the time of etching, such as the below-mentioned source drain.

[0023] n+ for taking ohmic contact with a source drain electrode on it Patterning is carried out so that the a-Si film 4 of a mold may be formed and it may be divided into a source and drain side. Patterning also of the a-Si film 5 which serves as a barrier layer which carried out continuation membrane formation previously in that case is carried out to coincidence. And n+ He forms a source drain electrode on the a-Si film 4 of a mold, and is trying to obtain a thin film transistor.

[0024]

[Effect of the Invention] Since according to this invention what added Cu or nickel to aluminum as a gate electrode and wiring is used based on the result obtained by experiment of this invention persons as explained in full detail above, the flatness and the gate

electrode which is easy to anodize which a hillock does not generate can be offered.

[Translation done.]

JAPANESE [JP,06-260642,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

* NOTICES *

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[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view of the thin film transistor of reverse stagger structure.
[Drawing 2] It is drawing showing the surface roughness and the sheet resistance by Cu addition of aluminum.
[Drawing 3] It is the insulating property Fig. of an oxide film on anode.
[Description of Notations]
1 Source Electrode
2 Drain Electrode
3 Protective Coat
4 N+ A-Si Film of Mold
5 A-Si Film
6 Insulator Layer
7 Oxide Film on Anode
8 Aluminum-1Wt%Cu Gate Electrode
9 Glass

[Translation done.]

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(43)公開日　平成６年(1994)９月16日

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		9056－4M	Ｈ０１Ｌ　29/ 78	３１１　Ｇ	

審査請求　未請求　請求項の数１　ＯＬ　（全　４　頁）

(21)出願番号　特願平5－47753

(22)出願日　平成５年(1993)３月９日

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愛知県刈谷市昭和町１丁目１番地　日本電装株式会社内
(72)発明者　恩田　正一
愛知県刈谷市昭和町１丁目１番地　日本電装株式会社内
(72)発明者　牧野　義典
愛知県刈谷市昭和町１丁目１番地　日本電装株式会社内
(74)代理人　弁理士　碓氷　裕彦

最終頁に続く

(54)【発明の名称】　薄膜トランジスタ

(57)【要約】
【目的】　ヒロックがなく平坦なゲート電極・配線を有する薄膜トランジスタを提供する。
【構成】　Ａｌに Ｃｕを１％添加した合金材料（以下Ａｌ－Ｃｕ）は表面粗さがＡｌだけの材料よりも約１／５，Ａｌに Ｓｉを１％添加した材料よりも約１／４と非常に平坦な金属表面が得られ、抵抗値もＡｌだけの材料より１．５倍程度と低い値が得られた。この抵抗値は配線材料として実用上問題にならない。またこの材料を陽極酸化しその上に絶縁膜を堆積し２層構造の絶縁膜とした場合にはＡｌの陽極酸化層を有する２層構造の絶縁膜に比べ絶縁特性は僅かに劣るものの同じ膜厚の１層の絶縁膜に比べ十分優れている。このＡｌ－Ｃｕ材料を逆スタガ構造の薄膜トランジスタのゲート電極・配線に使用することにより絶縁特性も十分でヒロックの発生しない平坦かつ低抵抗となるゲート電極・配線となり、薄膜トランジスタとして歩留り良く信頼性の高いものが得られる。

【特許請求の範囲】
【請求項１】　絶縁性基板と、
該絶縁性基板上に部分的に設けられたＣｕあるいはＮｉが添加されたＡｌからなるゲート電極およびゲート配線と、
該ゲート電極の表面を陽極酸化した第１絶縁層と、
該第１絶縁層を覆うように前記絶縁性基板上に設けられた第２絶縁層と、
該第２絶縁層上に設けられた半導体層と、
該ゲート電極の両側に沿うように該半導体層上に設けられたソース領域およびドレイン領域と、
を有することを特徴とした薄膜トランジスタ。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、液晶表示パネル等に用いられる逆スタガ構造の薄膜トランジスタ（以下ＴＦＴという）に関するものである。
【０００２】
【従来技術】従来、ＴＦＴのゲート電極としては基板との接着性が良いこと、表面にヒロックと呼ばれる凹凸がないこと、ゲート絶縁膜であるＳｉＮを形成する過程で変質しないことが条件になっており、Ｃｒ膜が使用されている。一方、ゲート配線としては抵抗の低いことが条件となり、固有抵抗率が高いＣｒ膜を流用することは適さない。そのため、Ｃｒ膜の上に固有抵抗率がＣｒよりも一桁以上低いＡｌ膜を重ねた２層膜が使用されている。
【０００３】しかしながら、このようにＴＦＴのゲート電極，配線に異なる構造を適用すると、パターニング工程数、すなわちマスク工程の増加をもたらすといった問題点がある。
【０００４】そこで、特開平２－８５８２６号公報に示される如く、ゲート電極・配線にＡｌもしくはＡｌ－Ｓｉ，Ａｌ－Ｐｄを用い、該ゲート電極・配線を陽極酸化してゲート絶縁膜の一部となし、その後ＳｉＮ等のゲート絶縁膜をプラズマＣＶＤにより成膜する方法が提案されている。
【０００５】
【発明が解決しようとする課題】しかしながら、ゲート電極に用いられるＡｌ，Ａｌ－Ｓｉ，Ａｌ－Ｐｄには以下に示すような問題がある。
【０００６】Ａｌはにヒロックとよばれる凹凸が発生しやすく、このヒロックによりゲート電極上に絶縁物を介して形成したチャネルの部分にも凹凸が発生する。そしてこの凹凸の部分で電子がチャネルを移動する距離が長くなり、電子移動度が低下しそれによりＴＦＴのスイッチング速度が遅くなるといった問題がある。
【０００７】Ａｌ－ＳｉはＡｌに比べヒロックが発生しにくいが、Ａｌ－Ｓｉを成膜後のパターニング工程においてＡｌ－Ｓｉ膜の除去されるべき箇所においてＳｉがエッチングされず残ってしまい、そのまま表示用画素を形成した場合、これが信号入出力の配線を短絡してしまうことがあり、表示用画素として機能しないといった問題がある。
【０００８】Ａｌ－ＰｄはＰｄが陽極酸化されにくくそのまま残ってしまい、その上にＳｉＮとａ－Ｓｉとをプラズマ ＣＶＤ法により成膜すると、酸化されなかったＰｄの部分で絶縁耐圧が下がり、ゲート電極・配線とその他の電極・配線とが短絡してしまいトランジスタとして機能しなかったり、故障の原因となるといった問題点があげられる。そのためこれらの金属材料をゲート電極・配線に用いた場合には、逆スタガ構造の薄膜トランジスタとして歩留りが悪く信頼性の低いものになってしまうといった問題が発生する。
【０００９】そこで本発明は上記問題点に鑑み、ヒロックが発生しにくく平坦なかつ陽極酸化されやすいゲート電極・配線を提供するものである。
【００１０】
【課題を解決するための手段】すなわち、上記課題を解決するためになされた本発明の薄膜トランジスタでは、絶縁性基板と、該絶縁性基板上に部分的に設けられたＣｕあるいはＮｉが添加されたＡｌからなるゲート電極およびゲート配線と、該ゲート電極の表面を陽極酸化した第１絶縁層と、該第１絶縁層を覆うように前記絶縁性基板上に設けられた第２絶縁層と、該第２絶縁層上に設けられた半導体層と、該ゲート電極の両側に沿うように該半導体層上に設けられたソース領域およびドレイン領域とを有することを特徴とする。
【００１１】
【実施例】本発明の一実施例である薄膜トランジスタのゲート電極・配線材料を以下に説明する。
【００１２】まず、ゲート電極・配線に使用する材料として従来どおり固有抵抗率の小さいＡｌを主体とする電極材料を使用することにした。そしてＡｌへの添加金属としてはＣｕとＮｉを選択した。これを以下に説明する。
【００１３】通常、電極・配線に電圧がかかると電子の流れにより電流が発生するが、Ａｌ電極・配線の場合、電子の流れの他にＡｌイオンの移動も電流に関与してしまう。このＡｌイオンの移動により電極あるいは配線が断絶してしまうことがある。これをエレクトロマイグレーションと呼ぶが、Ｃｕはこのエレクトロマイグレーションに対して有効であることが知られている。
【００１４】またＮｉにおいてはヒロック発生抑止に効果のあることが知られている。次にそれらについてヒロックの目安となるＡｌへの添加による表面粗さと、信号遅延の原因となるシート抵抗値を調べた。その調査結果を前記特開平２－８５８２６号公報に挙げられているＡｌ，Ａｌ－Ｓｉ（Ｓｉ１％）の調査結果とともに表１に示す。なお、調査した材料はＡｌだけの純Ａｌ，Ｓｉが

１％添加されたＡｌ－1wt%Ｓｉ，Ｃｕが１％添加されたＡｌ－1wt%Ｃｕ，Ｎｉが３％添加されたＡｌ－3wt%Ｎｉである。

【００１５】

【表１】

	純Al	Al-1wt%Si	Al-1wt%Cu	Al-3wt%Ni
平均表面粗さ Ｒａ（ｎｍ）	１３．１	９．５	２．６	３．８
シート抵抗 ）（膜厚200nm（Ω／□）	０．１９	０．５４	０．２９	０．５３

この表１によると表面粗さは純Ａｌでは１３．１ｎｍ、Ａｌ－1wt%Ｓｉでは９．５ｎｍであることに対しＡｌ－1wt%Ｃｕでは２．６ｎｍ、Ａｌ－3wt%Ｎｉでは３．８ｎｍとなっておりＡｌ－1wt%Ｃｕは表面粗さが純Ａｌだけのものよりも約１／５，Ａｌ－1wt%Ｓｉだけのものよりも約１／４と非常に平坦な金属表面が得られた。またＡｌ－3wt%Ｎｉにおいても表面粗さは純Ａｌだけのものよりも約３／１０，Ａｌ－1wt%Ｓｉだけのものよりも２／５と非常に小さくなっていることが分かる。これにより、ＡｌにＣｕあるいはＮｉを添加した電極はＡｌだけの電極やＡｌにＳｉを添加した電極よりも非常に良いといえる。

【００１６】またシート抵抗についてはＡｌ－1wt%Ｃｕは約１．５倍程度となりＡｌに比べほとんど差はないといえる。また、Ａｌ－1wt%ＳｉとＡｌ－3wt%Ｎｉはほぼ同程度であり純Ａｌに比べ約３．６倍と大きい値になるが一桁も異なるということではないのでＡｌ－3wt%Ｎｉもほぼよい値とみなせる。このシート抵抗の増大は$CuAl_2$などの化合物の形成や不純物散乱による抵抗率の増大のためと考えられる。したがってシート抵抗値については純Ａｌに比べＡｌ－1wt%Ｓｉ，Ａｌ－3wt%Ｎｉ，Ａｌ－1wt%Ｃｕはそれぞれ劣るものの実用上あまり問題ないとみなせる。特にＡｌ－1wt%Ｃｕのシート抵抗値はＡｌのシート抵抗値にかなり近い値を示したためＡｌ－1wt%Ｓｉ，Ａｌ－3wt%Ｎｉに比べ非常に良いといえる。

【００１７】以上の結果に基づき、次にＡｌに添加するＣｕの最適添加量を調べてみた。その結果を図２に示す。このときのＡｌ－Ｃｕ膜厚は２００ｎｍとした。この図より表面粗さはＣｕが１％のときが２．６ｎｍと最良である。またシート抵抗は添加量の増加につれて大きくなることがわかる。従って、表面粗さが小さくシート抵抗も小さいといった２つの要望を満たす最適の添加量は１％となる。このときのシート抵抗は前記の通り純Ａｌの場合の１．５倍とわずかに大きくなるが配線材料として実用上問題になるほどではない。

【００１８】次にＡｌにＣｕを１％添加したＡｌ－1wt%Ｃｕ薄膜を陽極酸化した膜の絶縁特性を調べた。その結果を図３に示す。Ａｌ－1wt%Ｃｕ薄膜を陽極酸化した膜と、Ａｌの陽極酸化膜との上にプラズマＣＶＤによりSiN_X膜をそれぞれ堆積させたものと、SiN_X膜だけのものとの絶縁特性をそれぞれ特性Ｘ，Ｙ，Ｚとして図３に示す。陽極化成液には０．１Ｍアジピン酸をアンモニア水にてｐＨ７．０±０．５に中和した水溶液を用いた。膜厚は４００ｎｍ一定とした。この図よりＸはＹに比べやや劣るが、Ｚに比べると一桁程度良い特性が得られた。これによりＡｌ－1wt%Ｃｕの陽極酸化膜は絶縁膜として十分にその機能を果たすといえる。

【００１９】このようにゲート電極としてＡｌにＣｕを１％添加したＡｌ－1wt%Ｃｕを用いれば、非常に平坦で抵抗も十分低い電極が得られる。またこのＡｌ－1wt%Ｃｕを陽極酸化しその上にSiN_X膜を堆積させたゲート絶縁膜も十分な絶縁特性を示す。

【００２０】以上のように、ヒロックの発生しない平坦な電極表面が得られ陽極酸化されやすいゲート電極と低抵抗なゲート配線となるようなＡｌにＣｕを１％添加したＡｌ－Ｃｕ材料をゲート電極・配線に用いることにより、より信頼性が高くまた歩留りのよい薄膜トランジスタを提供できる。

【００２１】以下に上記のゲート電極・配線材料を用いた薄膜トランジスタの一製造工程例を図１に簡単に示す。なお、この図にはゲート配線は示されていないがゲート電極のパターニング時に同時にパターニングされるものである。

【００２２】ガラス基板９にゲート電極８となるＣｕが１％添加されたＡｌ－1wt%Ｃｕを堆積し所望のパターンにパターニングする。パターニングされたゲート電極８の表面を０．１Ｍアジピン酸をアンモニア水にてｐＨ７．０±０．５に中和した水溶液により陽極酸化し陽極酸化膜７を成膜する。この陽極酸化はゲート電極８上にたとえゴミが存在していても陽極酸化液がその下に回り込むため絶縁膜となる陽極酸化膜７を確実に成膜することができる。陽極酸化膜７上にＳｉＮからなる絶縁膜６およびチャネルとなるａ－Ｓｉ膜５，さらにＳｉＮからなる保護膜３をプラズマＣＶＤにより連続成膜する。そ

して保護膜３だけをパターニングする。この保護膜３は後述のソース・ドレイン等のエッチングの時のエッチャントからチャネル層であるａ－Ｓｉ膜５を保護する役割をする。

【００２３】その上にソース・ドレイン電極とのオーミックコンタクトをとるためのｎ$^+$型のａ－Ｓｉ膜４を成膜しソース側、ドレイン側に分かれるようにパターニングする。その際、先に連続成膜した活性層となるａ－Ｓｉ膜５も同時にパターニングする。そしてｎ$^+$型のａ－Ｓｉ膜４上にソース・ドレイン電極を形成して薄膜トランジスタを得るようにしている。

【００２４】

【発明の効果】本発明によると、以上詳述したように本発明者らの実験により得られた結果に基づき、ゲート電極・配線としてＡｌにＣｕあるいはＮｉを添加したものを用いているため、ヒロックが発生しない平坦かつ陽極酸化されやすいゲート電極を提供できる。

【図面の簡単な説明】

【図１】逆スタガ構造の薄膜トランジスタの断面図である。

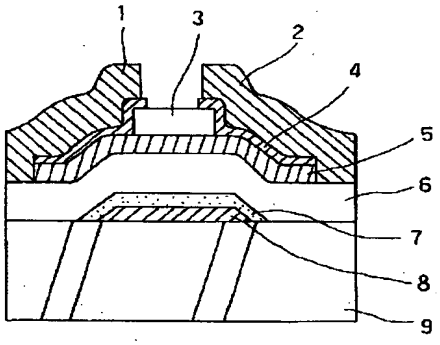
【図２】ＡｌのＣｕ添加量による表面粗さとシート抵抗値を表す図である。

【図３】陽極酸化膜の絶縁特性図である。

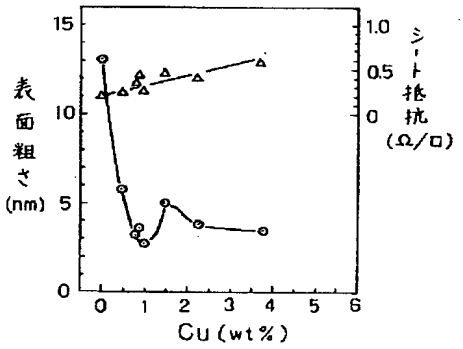
【符号の説明】

1　ソース電極
2　ドレイン電極
3　保護膜
4　ｎ$^+$型のａ－Ｓｉ膜
5　ａ－Ｓｉ膜
6　絶縁膜
7　陽極酸化膜
8　Ａｌ－1wt%Ｃｕゲート電極
9　ガラス

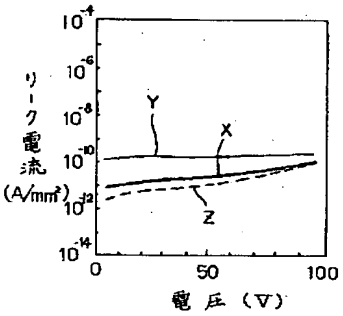
【図１】



【図２】



【図３】



フロントページの続き

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